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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,205	09/24/2003	Sarah E. Kim	ITL.1040US (P14807)	2630

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,205	KIM ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,14 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14,16 and 17* is/are allowed.

6)☒ Claim(s) *1,3-7 and 18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 3/20/06. Currently, claims 1, 3-7, 14 and 16-21 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The rejection of claims 1 6 and 7 under 35 U.S.C. 103(a) as being unpatentable over Jankowski et al., Patent Application Publication US 2004/0072039 in view of Vaiyapuri US Patent 6,629,425 has been maintained for reasons of record.

Jankowski discloses the semiconductor method substantially as claimed. See figures 1-11, and corresponding text, where Jankowski teaches, pertaining to claim 1, a method comprising: forming a trench **906** (host structures) in each of two semiconductor substrates (figures 5, 9 and 10; paragraphs [0023], [0025] and [0045-0046]); providing a catalyst **904** in a trench (figures 9 and 10; paragraph [0044-0046]); and combining said substrates in a face-to-face abutment with said trenches (host structures) in alignment with one another (figures 9 and 10; paragraph [0029] and [0044-0046], ***Note***: the Examiner takes the position that the substrates are in a face-to-face abutment, since Jankowski teaches, that the host structure consists of silicon wafers that have channels (implied trenches) etched within the silicon wafers, and are bonded together to form flow channels). In addition, Jankowski shows, pertaining to claim 6, the

method including depositing the catalyst in the trench (figure 9; paragraph [0044]). Finally, Jankowski shows, pertaining to claim 7, the method including depositing platinum or lead in said trench (figure 9; paragraph [0045] platinum).

However, Jankowski falls to show, pertaining to claim 1, forming a trench in each of two semiconductor substrates, at least one of said trenches extending completely across one of said semiconductor substrates from edge to edge.

Vaiyapuri teaches, in figures 1A-12, and corresponding text, a similar method of forming a trench in each of two semiconductor substrates, at least one of said trenches extending completely across one of said semiconductor substrates from edge to edge (col. 5, lines 5-17; col. 6, lines 18-47).

It would have been obvious to one of ordinary skill in the art to substitute, forming a trench in each of two semiconductor substrates, at least one of said trenches extending completely across one of said semiconductor substrates from edge to edge, in the method of Jankowski, pertaining to claim 1, according to the teachings of Vaiyapuri, with the motivation of cooling the integrated circuits so as to prevent damage to semiconductor devices.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The rejection of claims 3-5 and 18-21 under 35 U.S.C. 103(a) as being unpatentable over Jankowski et al., Patent Application Publication US 2004/0072039 in view of Vaiyapuri US Patent 6,629,425, in further view of Burgess et al., US Patent 5,293,070 has been maintained for reasons of record.

Jankowski in view of Vaiyapuri, discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1, 6 and 7 under 35 U.S.C. 103(a). In addition, Jankowski in view of Vaiyapuri shows, pertaining to claim 18, a method comprising: and defining a catalyst-filled **904** trench between said substrates (figures 9 and 10; paragraph [0044-0046]). Finally, Jankowski in view of Vaiyapuri shows, pertaining to claim 21, including forming a trench in each of said semiconductor substrates ([0023], [0025] and [0045-0046]).

However, Jankowski in view of Vaiyapuri fails to show, pertaining to claims 3 and 18, including combining said (two semiconductor substrates) substrates using copper-to-copper bonding. In addition, Jankowski in view of Vaiyapuri fails to show, pertaining to claims 4 and 19, including masking said catalyst to avoid coating the catalyst with the copper. Finally, Jankowski in view of Vaiyapuri fails to show, pertaining to claims 5 and 20, including lifting off a resist to remove the copper from the catalyst.

Burgess teaches, in figures 1-6, and corresponding text, a method for bonding two substrates using copper-to-copper bonding where a fluid conductor element that include micro-channels are bonded to top and bottom plates (col.6, lines 46-61).

It would have been obvious to one of ordinary skill in the art to substitute the following steps of: including combining said (two semiconductor substrates) substrates using copper-to-copper bonding; including masking said catalyst to avoid coating the catalyst with the copper;

including lifting off a resist to remove the copper from the catalyst, in the method of Jankowski in view of Vaiyapuri, pertaining to claims 3-5 and 18-20, according to the teachings of Burgess, with the motivation that since copper has very low resistance, and that it can bond at lower temperatures, bonding the substrates with copper, would result in more efficient bonding technique. Finally, it would be obvious to protect the catalyst with a mask to avoid the copper coating, with the motivation of, only placing the copper within the bonding regions of the substrates to perform the copper to copper bonding of the two substrates.

Allowable Subject Matter

Claims 14, 16 and 17, are allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

The closest prior art of record, Jankowski et al. Patent Application Publication US 2004/0072039, taken alone or in combination with Vaiyapuri US Patent 6,629,425 and Burgess et al, US Patent 5,293,070, fails to show the following steps:

Pertaining to independent claim 14, "protecting said catalyst when forming said channels."

Response to Arguments

Applicant's arguments filed 3/20/06 have been fully considered but they are not persuasive. In the Remarks on pages 4 and 5:

The Applicant raises the clear issue as to whether Vaiyapuri suggests, that trenches extend completely across one of the semiconductor substrates from edge to edge. In addition, the Applicant raises the clear issue as to whether Burgess suggests copper-to-copper bonding.

The Examiner takes the position that based on the implications of Jankowski, alone with the solid teachings of Vaiyapuri, one of ordinary skill in the art would have substituted the channel arrangements taught by Vaiyapuri into the Jankowski channel arrangements. In addition, based on the combined solid teachings of Jankowski in view of Vaiyapuri, one of ordinary skill in the art would have included the copper-to-copper bonding step taught by Burgess. Specifically, Jankowski shows that two semiconductor substrates are aligned in face-to-face abutment (figures 9 and 10; [0029] and [0044-0046]). It takes the solid teachings of Vaiyapuri to provide the motivation of forming the channels (trenches) to be edge-to-edge, for the purpose of cooling the integrated circuits so as to prevent damage to the semiconductor devices. With regards to whether Vaiyapuri teaches the channels to extend from edge to edge is shown in figures 9A-10B, where as stated in col. 8, lines 40-53, that fluids are pumped sequentially through the cavities and interconnected cooling channels. Therefore, one of ordinary skill in the art would conclude that the channels are formed from edge to edge, since the fluids are clearly passing through the channels and the cavities sequentially.

Based on the combined teachings of Jankowski in view of Vaiyapuri, Burgess supplies the motivation to using a copper-to-copper bonding techniques, with the advantages that copper has a very low resistance, and that it can bond at lower temperatures proving to be a more efficient bonding process. With regards to whether Burgess teaches copper-to-copper bonding is stated in col. 4, lines 10-15, 30-37 and 55-65, that the top plate and bottom plates are made of

copper or a copper alloy in which the block that includes the channel elements are sandwiched between the two plates. Therefore, one of ordinary skill in the art would conclude that a copper-to-copper bonding technique is performed.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
May 23, 2006

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